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# BEFORE THE BOARD OF PATENT APPEALS
# AND INTERFERENCES

Application Number: 09/133,741
Filing Date: August 13, 1998
Appellant(s): BALDWIN, DAVID ROBERT

Robert Groover
For Appellant

**EXAMINER'S ANSWER**

**(1)    Real Party in Interest**

A statement identifying the real party in interest is contained in the brief.

**(2)    Related Appeals and Interferences**

A statement identifying the related appeals and interferences which will directly affect or

be directly affected by or have a bearing on the decision in the pending appeal is contained in the

brief.

**(3)    Status of Claims**

The statement of the status of the claims contained in the brief is correct.

**(4)    Status of Amendments After Final**

The appellant's statement of the status of amendments after final rejection contained in

the brief is correct.

**(5)    Summary of Invention**

The summary of invention contained in the brief is correct.

**(6)    Issues**

The appellant's statement of the issues in the brief is correct.

**(7)    Grouping of Claims**

Appellant's brief includes a statement that claims 1, 11, 15-16, 21 and 48 do not stand or

fall together and provides reasons as set forth in 37 CFR 1.192(c)(7) and (c)(8).

**(8)    Claims Appealed**

The copy of the appealed claims contained in the Appendix to the brief is correct.

## (9)    *Prior Art of Record*

| 5,877,773 | Rossin et al | 3-1999 |
| 5,613,052 | Narayanaswami | 3-1997 |
| 5,361,386 | Watkins et al | 11-1994 |

Sutherland, Ivan E. "Micropipelines" Communications of the ACM, vol.32, no.6 (1989), pp. 720-738

## (10)    *Grounds of Rejection*

The following ground(s) of rejection are applicable to the appealed claims:

### *Claim Rejections - 35 USC § 103*

1.    The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2.    Claims 1-2, 7-11, 14-15, 48, 50-51 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rossin et al (U.S Patent No. 5,877,773) in view of Sutherland ("Micropipelines", Communications of the ACM, June 1989, volume 32, number 6).

As per claim 1, Rossin et al teaches a method for clipping graphics primitives. The method comprises the steps of: using a clipping algorithm with only one buffer 304 (fig.3 and 5A) to store input and output polygons of the primitive (fig.5A; col.8, lines 66-67 and col.11,

lines 48-51; col.12, lines 4-12; and col.4, lines 17-32); and indicating whether each vertices is visible in each plane (col.7, lines 58-65).

Rossin et al does not explicitly disclose using only one circular buffer for storing input and output vertices of a primitives. However, Sutherland suggests using a circular buffer to store clip data (page 720, last two lines of the first column; page 732, second column, section "Other Devices using the Same Protocol"; page 735, first column, first paragraph). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to replace the only one buffer of Rossin with a circular buffer of Sutherland. The motivation for this would have been to built a simple storage device capable or replacing oldest data with the newest data in clipping operation in which vector length are always changing.

As per claim 2, rasterizing only vertices which are visible in all planes would have been both well known and obvious to a person of ordinary skill in the art at the time the invention was made.

As per claim 7, using frustum view volume as clipping planes would have been well known to a person of ordinary skill in the art at the time the invention was made. It would have been an obvious choice to a person of ordinary skill in the art at the time the invention was made to use the well known frustum volume instead of the clipping planes of Rossin et al in order to perform view clipping using the Sutherland Hodgman clipping method of Rossin et al.

As per claim 8-10, Rossin et al teaches there are six planes in view volume (col.3, lines 31-36). Further, including more than six view planes would have been obvious to an ordinary person skilled in the art at the time the invention was made as taught by Rossin (col.7, lines 45-50). It would have been obvious to a person of ordinary skill in the art at the time the invention was made to include more than six planes in the view volume, since increasing the number of viewing plane and adjusting the size of the circular buffer require only routine skill in the art.

As per claim 11, Rossin et al teaches Sutherland and Hodgman clipping algorithm (col.19, lines 53-58).

As per claim 14, Sutherland does not explicitly disclose using two circular buffers to store input and output polygons. However, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to integrate duplicate circular buffer of Sutherland, because integrating duplicated circular buffer together involves only routine skill in the art (St. Regis Paper Co. v.bennis Co., 193 USPQ 8).

As per claim 15, Rossin et al teaches a buffer with maximum storage of sixteen vertices (from I0-07 in Fig.5A).

As per claim 48, refer to discussion in claim 1 above. Further, Rossin et al discloses a computer system with well known display hardware (col.1, lines 24-26, lines 60-61); a processor

108 (fig.1) connected to provide graphic data (col.6, lines 52-54); a geometry 120 (fig.2) and

lighting accelerator 202 (fig.2) (col.7, lines 21-22, and line 52) with a transformation unit 200

(fig.2) (col.7, lines 51-52, lines 55-65); a geometry unit 120 (fig.2) which performs clip testing,

clipping the primitives, outputting a view clip code, and outputting clipped graphic data to be

rendered (col.7, lines 58-67; col.8, lines 1-8); moreover, Rossin et al discloses a well known

video rendering hardware for generating and displaying graphics (col.1, lines 41-44, 60-61).

      As per claim 50, Rossin et al teaches polygon and triangle primitive (col.1, lines 24-33).

      As per claim 51, refer to discussion in claims 11 above.

3.      Claims 16-17, 20-24, 26-27, 47 are rejected under 35 U.S.C. 103(a) as being unpatentable

over Rossin et al (U.S Patent No. 5,877,773) in view of Sutherland ("Micropipelines",

Communications of the ACM, June 1989, volume 32, number 6) and further in view of Watkins

et al (U.S Patent No. 5,361,386).

      As per claim 16, 47, refer to discussion in claims 1 above. Rossin et al does not disclose

defining all vertices of a primitive using relational coordinates.  However, Watkins in the same

computer graphic field of endeavor (col.6, lines 10-17) teaches defining all vertices of a

primitive using relational coordinates as claimed (col.9, lines 66-68 and col.10; and col.11). It

would have been obvious to a person of ordinary skill in the art at the time the invention was

made to define the vertices of a primitive in barycentric coordinate as taught by Watkins et al in

the clipping method of Rossin et al. The motivation for this would have been to facilitate

interpolation to determine the color and light of the intercepted points of the clipping planes as

taught by Watkins in col.8, lines 56-58 and to prevent converting vertices coordinates from one

coordinate to another coordinate system in clipping, texturing and light shading procedure.

As per claim 17, 22-24, 26-27, refer to discussion in claims 2, 7-8, 11, 14-15 above.

As per claim 20, Rossin et al discloses polygon and triangle primitive (col.1, lines 24-33).

As per claim 21, Watkins teaches barycentric relational coordinates (abstract).

4.      Claims 3, 12-13, 49, 52, are rejected under 35 U.S.C. 103(a) as being unpatentable over

Rossin et al (U.S Patent No. 5,877,773) in view of Sutherland ("Micropipelines",

Communications of the ACM, June 1989, volume 32, number 6) and further in view of

Narayanaswami (U.S Patent No. 5,613,052).

As per claim 3, 49, Rossin et al does not discloses performing clipping prior to lighting or

texture calculation.  However, Narayanaswami teaches performing clipping prior to lighting or

texture calculation (col.1, lines 12-25, lines 53-67).  It would have been obvious to a person of

ordinary skill in the art at the time the invention was made to perform clipping before lighting

and texture calculation. The motivation for this would have been to reduce computational

requirements and increasing rendering speed by clipping the data that lies outside the field of

vision as motivated by Narayanaswami in col.1, lines 15-25.

As per claim 12-13, 52, Narayanaswami discloses indicating vertex visibility by a bit flag

(col.5, lines 44-67; and col.6, lines 1-14). Narayanaswami does not teach 12 bit visibility flag.

However, Narayanaswami teaches selecting the number of the visibility bit flag according to the

number of non-overlapping region (col.5, lines 44-52).  It would have been obvious to a person

of ordinary skill in the art at the time the invention was made to select the twelve bit flag when

the twelve clipping planes of Rossin et al is used.

5.      Claims 18, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Rossin et al

(U.S Patent No. 5,877,773) in view of Sutherland ("Micropipelines", Communications of the

ACM, June 1989, volume 32, number 6) and further in view of Watkins et al (U.S Patent No.

5,361,386) and Narayanaswami (U.S Patent No. 5,613,052).

As per claim 18, 25 refer to discussion in claims 3, 12 above.

## (11)   Response to Argument

- Issue #1:  in page 11, third paragraph, the appellant discuss the primary reference

    Rossin et al 5,877,773.  However, the appellant does not provide any

    specific argument concerning Rossin et al's teaching.  Instead, the appellant

    just cite the examiner's comment that Rossin does not teach using only one

circular buffer for storing input and output vertices". The following is the examiner comment:

- Response #1: The appellant fails to go in depth to the teaching of the memory device 304 (fig.3) of Rossin, the appellant, therefore, ignores very important teaching of Rossin concerning using only one memory to store both input and output vertices of a primitive. As seen in fig.5A, the memory device 304 (fig.3 and 5A) stores input and output coordinate of the vertices before and after clipping (col.8, lines 66-67; col.11, lines 48-51; col.12, lines 4-12). Note that there is another memory device 306 (fig.3 or fig.5B), however, this memory device 306 (fig.3 or 5B) does not store both input and output vertices of a primitive, therefore this memory device 306 (fig3) should not be considered as a second memory that stores both input and output vertices. Since _only the memory device 304 (fig.3 or fig.5A) stores input and output vertices of a primitive_ (a triangle in fig.4A), Rossin clearly teaches using _only one memory device 304 (fig.3 or 5A) to stores input and output vertices on a primitive_. Although Rossin does not explicitly teach that the memory device 304 (fig.3 or 5A) should a ring buffer, the capability of shifting vertices from the input list location to the output list location taught in col.12, lines 4-8 with reference to fig.5A suggests a circular buffer. The secondary literary of Sutherland suggests using circular buffer in

clipping process. This secondary document of Sutherland as well as the
suggestion to combine teaching of Rossin and Sutherland will be
discussed in the response #2 below.

- Issue #2: in page 11, last paragraph through page 13, two first paragraphs, the
appellant admits that Sutherland does suggest the use of circular buffers in
connection with clipping operations (page 12, lines 3-4, and page 13,
second paragraph: "Thus Examiner Nguyen is correct ... in connection with
clipping" of the appeal brief). However, the appellant asserts that Clipping
using Sutherland and Hodgman algorithm requires two separate buffers for
holding input and output vertices of polygons and that Sutherland does not
suggest combining two circular buffers into one. (It is important to note
that the accidental coincident name "Sutherland" in "Sutherland and
Hodgman algorithm" should not be mistakenly thought that it is the
algorithm taught in the cited non-patent document of Sutherland. The
"Sutherland and Hodgman algorithm" (note that there must be the name
Hodgman going side by side with the Sutherland) is just a well known
clipping technique commonly used in computer graphics to clip a polygon
against a view plane. The "Sutherland and Hodgman algorithm" is not
taught in the cited literary "micropipelines" of Sutherland. Rossin does
mention using such the well known "Sutherland and Hodgman algorithm"
in his clipping technique in col.19, lines 53-57; col.2, lines 40. When the

name "Sutherland" is used alone, the examiner refers to the teaching of

Sutherland in the cited non-patent literary "Micropipelines"). The following

is the examiner's answer:

- <u>Response #2</u>: Sutherland basically teaches implementation of a micropipeline, which

  is basically just a first-in-first-out (FIFO) memory device (page 720,

  last three lines of column 1). Sutherland further suggests that the

  micropipeline can be replaced with a ring buffer (page 732, first

  paragraph of the section "Other devices using the same protocol" in the

  second column). Therefore Sutherland teaches using a ring buffer as a

  memory device as admitted by the appellant. In page 735, first

  paragraph of column 1, Sutherland further teaches using the

  micropipeline (which is the ring buffer) in clipping operation where the

  vector length changes. Refer back to fig.5A of Rossin (US 5,877,773),

  it is clear that the teaching of Rossin has 2 important features that fit in

  the teaching of Sutherland and that makes replacing such the only one

  memory device 304 (fig.3 and 5A) with the only one ring buffer of

  Sutherland obvious to an ordinary person at the time the invention was

  made. (1) First, the memory device 304 (fig.3 and 5A) of Rossin is <u>*the*</u>

  <u>*only one*</u> memory device that stores both input and output vertices, and

  that can shift data from one memory location (the output list location) to

  another location (the input list location) (Rossin col.12, lines 4-8), this

feature clearly suggests a characteristic of a circular buffer. Since the

ring buffer of Sutherland is just one memory device capable of shifting

data within the ring buffer, replacing the only one memory 304 (fig.3 or

5A) with the only one ring buffer would have been possible. (2)

Second, the *only one* memory device 304 (fig.3 and 5A) is *used in*

*clipping process*, *and* note that the memory device 304 (fig.3 and 5A)

*stores varied length vectors* (V0 V1 V2), (V4 V1 V2 V5), (V4 V6 V7

V2 V5), etc. with the length of 3, 4, and 5, etc. elements respectively.

The characteristic and functionalities of the memory device 304 (fig.3

and 5A) fit exactly with the suggest application of the ring buffer of

Sutherland in page 735, first paragraph, first column. Replacing the

only one memory device 304 (fig.3 and 5A) that functions exactly the

same as the ring buffer of Sutherland can perform as disclosed in

Sutherland's page 735, first paragraph, first column is clearly within the

knowledge of a person of ordinary skill in the art. Contrary to the

appellant assertion that clipping using "Sutherland and Hodgman

algorithm" needs two separate buffers for holding input and output

vertices of polygons, Rossin teaches using "Sutherland and Hodgman

algorithm" for clipping process (col.19, lines 53-58) *using only one*

*memory device 304* (fig.3 and fig.5A) for storing both input and output

vertices of primitives (Rossin col.8,lines 66-67; col.11,lines 48-51;

col.12, lies 4-12).  Further, there is no need to combine any two buffers

into one as asserted by the appellant in Rossin because Rossin simply

just teaches using only one memory device 304 (fig.3 &5A) for storing

both input and output vertices.

- Issue #3:  in page 13, last two paragraphs, the appellant roughly explains the

    references of Watkins (US 5,361,386), and Narayanaswami (US

    5,613,052).  The following is the examiner comment:

- Response #3: The appellant does not provide any specific argument concerning the

    application of the references to any specific claim, therefore, the

    examiner can not provide any specific response on this issue.  However,

    it should be noted that Watkins suggests using relational coordinates in

    computer graphics (refer to the response #6 (c) for further explanation

    concerning claim 16 and the combined teaching of Rossin and

    Watkins).  It should also be noted that Narayanaswami's teaching is

    within the same "clipping" field of endeavor (abstract; title) of Rossin.

    Narayanaswami suggests that recognizing clipping vertices should be

    performed prior to performing lighting or texture mapping for the

    unclipped vertices.  By determining clipping status of the vertices prior

    to performing lighting and texturing, computational resources can be

    greatly saved (Narayanaswami, col.1, lines 53-67; col.2, lines 1-12).

    An ordinary person skilled in the art at the time the invention was made

would be able to improve speed and to save the graphic computational

resources of the system of Rossin by performing clipping prior to

lightning or texture mapping.

- Issue #4: on page 14 through page 15 first paragraph, the appellant again asserts that

    there is no motivation to combine or modify the primary reference of

    Rossin and secondary reference of Sutherland for using only a single buffer.

    The following is the examiner response:

- Response #4: Replacing the only one memory 304 (fig.3 & 5A) of Rossin with the

    ring buffer taught by Sutherland is both suggested and obvious to an

    ordinary person skilled in the art at the time the invention was made.

    Refer to the response #2 above for more detailed explanation.

- Issue #5: In page 15, second paragraph, the appellant argues that no reference teaches

    using a circular buffer that has a maximum storage of sixteen vertices for

    permitting 12 clipping planes to be used as claimed in claim 15.  The

    following is the examiner's answer:

- Response #5: The combine teaching of Rossin and Sutherland suggest using a circular

    buffer 304 (fig.3 and 5A) to store vertices of primitives (refer to the

    response #2 above).  Rossin teaches the buffer 304 (fig.5A) capable of

    storing 16 vertices (counting from I0-I7 to 00-07, there are sixteen rows

    altogether, since each row stores one vertex, sixteen rows clearly stores

    sixteen vertices).  Moreover, although, for simplifying purpose, Rossin

teaches an easiest example of clipping on two dimensional objects using

4 clipping planes Xmin, Xmax, Ymin, Ymax (col.11, lines 36-38),

Rossin teaches that additional clipping planes can be implemented

(col.7, lines 45-50). Therefore, adjusting the size of the buffer to

accommodate more clipping planes as needed in a specific application

requires only routine skill in the art. It is also important to note that

claim 15 does not disclose the number of clipping planes, therefore

claim 15 concerning the size of the buffer holding sixteen vertices does

not highlight the fact that the single buffer size of the present

application is just haft that which would be used for conventional

buffer, therefore, the appellant's argument in this respect should not be

taken into consideration.

- Issue #6: In page 15 through page 16, section "grouping of claims", the appellent

    requests that the claims on appeal should not stand or fall together.

    However, the appellant just repeat the claim language and does not

    specifically provide any specific explanation concerning each single issue

    of the claim. The following is the examiner comment and explanation:

- Response #6:

    a. Concerning claim 11 and 24, Rossin teaches using "Sutherland and Hodgman

        algorithm" for polygon clipping (col.19, lines 53-58).

b.  Concerning claim 15, Rossin teaches a buffer size of 16 vertices in fig.5a. Moreover, refer to discussion in issue #5 above for detail analysis of the claim vs. Rossin's teaching.
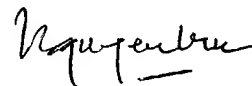
c.  Concerning claim 16, Rossin teaches calculating view clip code (col.7, lines 55-67; col.8, lines 1-32).  And the third cited reference of Watkins teaches utilizing relational coordinates in computer graphics involving polygon transformation, light shading, texture shading and clipping (abstract; col.6, lines 10-17) (note that the "Barycentric coordinates" is a specie of the generic "relational coordinate"). Watkins further teaches that the relational coordinates can be utilized in other computer graphic operations (col.25, lines 28-35).  Since Rossin teaches a computer graphic system capable of doing the same transformation, light shading, texture shading and clipping processes (Rossin, col.7, line 50-53; col.7, lines 1-12) as taught by Watkins, using relational coordinates to defines the vertices of polygons of Rossin as suggested by Watkins would have been obvious to an ordinary person skilled in the art at the time the invention was made in order to prevent distortion in interpolation process as taught by Watkins in col.8, lines 56-59 and at the same time to avoid changing vertices coordinate from one coordinate system to another coordinate system in the lighting and clipping process.

d.  Concerning claim 21, refer to claim 16 in section c. above.

e. Concerning claim 48, Rossin clearly discloses the well known units:

transformation unit 200 (fig.2) (col.7, line 51-52); a geometry unit 120 (fig.2)

(col.7, line 43-44); a video rendering hardware and display hardware (col.1, lines

41-44, lines 60-61, and line 25); and a processor 108 (fig.1) connected to provide

graphics data (col.6, lines 52-54).

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

**THU V. NGUYEN**
**PRIMARY EXAMINER**

July 5, 2004

Conferees:

1) Thomas Black

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